

Backplane Programming

The PL-1746 Programmable Limit Switch Module was designed to work in a SLC-500 series chassis. All of the module's channels, enable inputs, configuration data, and pulse information is available to the SLC-500 processor through the backplane of the chassis. All of the data in the PLS module accessible by the SLC-500 processor is contained in one of four data files. These are the Input file, Output file, M0 file, and M1 file. Each data element in these files is referred to in the ladder program by a specific address. Addresses are constructed as follows:

Addressing

F:S.R/B where:

F is the file specifier. It is I for input files, O for output files, M0 for the M0 files and M1 for the M1 files.

S is the number of the slot in which the PLS module is installed.

R is the desired register number.

B is the number of the desired bit in the specified register.

If you are accessing an entire register, the /B parameter is not needed. It is only used to access specific bits of a register. For instance, if the ladder program needs the resolver speed, and the PLS module is installed in slot three of the SLC-500 chassis, the ladder program would reference address M0:3.22. When the ladder program checks the status of the Any Error bit in the Programming Error Register, it would reference address I:3.7/15. Because this flag is a single bit, the /B parameter is required.

Input File

The input file in the PL-1746 module contains ten data words. The first two words (I:S.0-I:S.1) contain the status of all 32 of the PLS outputs. The next three words (I:S.2-I:S.4) in the input file are not pre-defined by the PLS. The Error Number Register is in I:S.6, and the Programming Error Register is in I:S.7. Raw Resolver Position, updated every scan cycle, is in I:S.8.

Output File

The output file also contains ten data words but only the first two words are pre-defined by the PLS. The first contains the Input Status Register. The PL-1746's six Group Inputs, the First Cycle Enable Input, and the Output Enable Input can be set or cleared by writing to O:S.0. The second word in the output file is the Active Program Register, O:S.1. This register controls which program in the PL-1746 is controlling the PLS outputs; if it contains zero, the program number in the Default Program register is used. Although data may be written to the eight other output file registers, it will be ignored by the PL-1746.

M0 & M1 Files

All PLS configuration data is accessed through the module's M0 file and all pulse data is accessed through the M1 file. Some registers in the M0 file are unused and are reserved for future expansion. All of the data in the M1 file, and most of the data in the M0 file, is stored in non-volatile memory and is retained during power down.

The M0 and M1 files are usually accessed through the use of a block transfer command such as MOV. In the PL-1746, the M1 file is read only. You can move a maximum of 1000 words with one block transfer. An error will be generated if a larger block size is attempted. The number of the last accepted register is placed in the error location register.

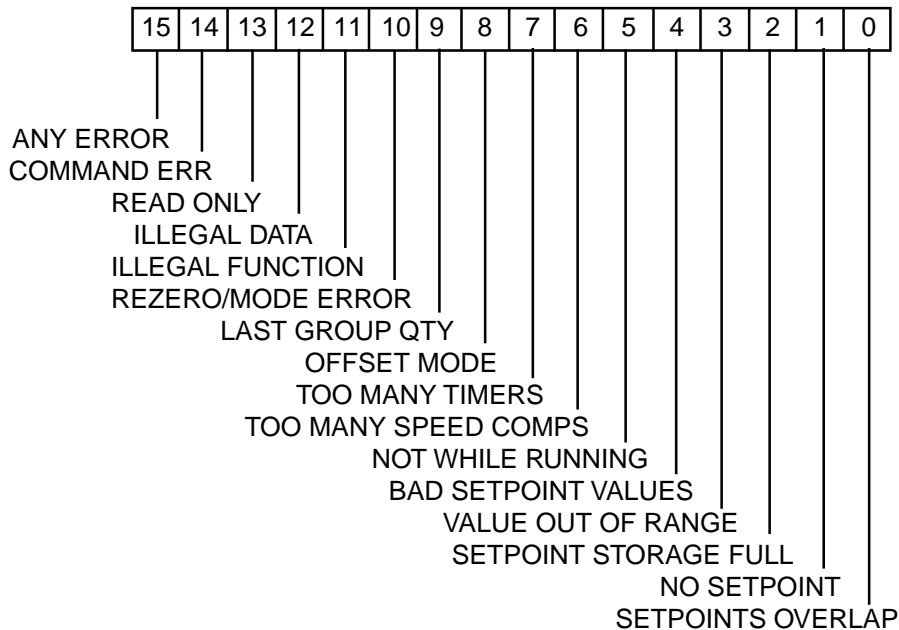
When the ladder program changes data in the M0 file, the change is checked for validity, and if valid, is stored in the non-volatile memory. After storing, the change takes effect. If the change is found to be invalid, the change is rejected, the Programming Error Register (I:S.7) is set to indicate the nature of the error, and the number of the register that generated the error is loaded into the Error Number Register (I:S.6). After making a change to the M0 file, the ladder program should test the status of the Programming Error Register. If an error was generated, the ladder program should correct the cause, and then clear the error by toggling the Clear Error bit (O:S.0/8) in the Input Status Register from 0 to 1.

Backplane Interlock

The PLS configuration data is stored in EE-PROM in the PL-1746. This type of non-volatile memory has very slow write cycles. Since the PL-1746 runs slower while storing configuration data than the SLC-500 ladder program, the possibility of backplane overflow exists. Also, in the C02/C03, copy commands should be limited to a maximum of 12 words, or the C02/C03 may cause a "specialty I/O module in slot 1 has not responded to a lock shared memory command within the required time limit" fault in the SLC program. To avoid these conditions, a register is available at M0:S.866 called Backplane Interlock. The ladder program writes a command or a series of commands to the PL-1746. It then writes a one to the backplane and tests that location to see when it changes back to zero. Whenever the PL-1746 detects a write to the Interlock, it will respond by writing zero back to that location. This allows the ladder program to know when the previous command has been executed. Then another command or series of commands can be delivered.

Backplane Programming (cont'd)

PROGRAMMING ERROR REGISTER (I:S.7)



PROGRAMMING ERROR REGISTER BITS:

- I:S.7/15 The ANY ERROR bit comes on if any other error bit in the Programming Error Register is turned on. No commands are executed if the ANY ERROR bit is on. To clear the ANY ERROR bit and the current error, toggle O:S.0/8 on and off. The errors are actually cleared on the rising edge of O:S.0/8. Then another error can be reported.
- I:S.7/14 The COMMAND ERR bit is set by an error from a programming command. The programming commands are Channel Copy, Program Copy, Pulse Copy and Pulse Edit.
- I:S.7/13 The READ ONLY error will be set if you write to a read only register.
- I:S.7/12 The ILLEGAL DATA error is reported when the specified data is out of the range permitted for that parameter.
- I:S.7/11 The ILLEGAL FUNCTION error is reported for all non-supported parameters.
- I:S.7/10 The REZERO/MODE ERROR is reported if an unsupported mode is specified.
- I:S.7/9 The LAST GROUP QTY error is reported when changing the quantity of the last group is attempted.
- I:S.7/8 The OFFSET MODE error is reported when changing the group mode to EACH while the group's mode is 1 or 2.
- I:S.7/7 The TOO MANY TIMERS error is caused by changing the timed output quantity to a value greater than four.
- I:S.7/6 The TOO MANY SPEED COMPS error by changing the quantity of speed compensated channels to a value greater than sixteen.
- I:S.7/5 The NOT WHILE RUNNING error is reported when attempting to change a variable that can only be changed when the machine is stopped.
- I:S.7/4 The BAD SETPOINT VALUES error is caused by creating or changing both edges of a pulse to a value other than 0 (deleting pulse) or 1 (ON all the time).
- I:S.7/3 The VALUE OUT OF RANGE error is reported when attempting to change a the contents of a variable to an excessive value.
- I:S7/2 The SETPOINT STORAGE FULL error will be reported if the non-volatile memory is full.
- I:S7/1 The NO SETPOINT error is reported if a command requires a pulse edge and none is provided.
- I:S7/0 The SETPOINTS OVERLAP error will be reported if a command results in on/off edges that overlap.

Backplane Programming (cont'd)

ERROR NUMBER REGISTER (I:S.6)

When an error is reported and the Any Error bit in the Programming Error Register is set, the register number of the command that caused the error is placed in the Error Number Register. This register is available from the PL-1746 in its input file at location I:S.6 (unless I:S.6 is mapped).

HARDWARE STATUS/ERROR REGISTER (I:S.5 - PL-1746-C02/C03 models only)

When a hardware fault error occurs, the PL-1746 turns off outputs, lights the Fault LED, shows a fault code on the local display, and indicates a fault by setting the Any Fault bit and a fault-specific bit in the Hardware Status/Error Register (I:S.5). The user must clear the fault via the Clear Error bit (O:S.0/8), or via turning the SLC-500 keyswitch to PROG and back to RUN. If the fault condition remains, it will again be flagged in the same manner. In all cases, the Hardware Status/Error Register is only updated if it's unmapped. An error message appears on the keypad/display, but clearing it has no effect on the internal status of the fault.

The Hardware Status/Error Register bits are defined as follows:

<u>Bit</u>	<u>Local Display</u>	<u>Description</u>
15	----	Any Fault
14	EX0F	Reserved
13	EX0E	System Busy
12	EX0D	I/O power supply failed
11	EX0C	SLC queue overflow
10	EX0B	SLC access timer time-out
9	EX0A	SLC fatal error
8	EX09	SLC interface pipe is full
7	EX08	SLC backplane overflow
6	EX07	Resolver not ok
5	EX06	NMI without PWRFAIL_
4	EX05	Interrupt from unused vector
3	----	Reserved
2	----	Reserved
1	----	Reserved
0	----	Reserved

The SLC program should assume the C02 is not ready for data whenever the System Busy bit is set. This can happen, for example, during startup and when the user changes scale factor. Unlike the other status bits, the System Busy bit and the Any Error bit (I:S.5/15) cannot be cleared by the SLC program; in this instance these bits are cleared by the C02 only. Also, when the system is busy, it doesn't turn off outputs, doesn't light the fault LED, and doesn't show anything on the local display. The SLC program should be continuously monitoring both the Programming Error Register's Any Error bit (I:S.7/15) and the Hardware Status/Error Register's Any Error bit, and taking appropriate action if either is set.

INPUT STATUS REGISTER 0:S.0

0:S.0/15	0:S.0/14	0:S.0/13	0:S.0/12	0:S.0/11	0:S.0/10	0:S.0/9	0:S.0/8
						Clear Shift Reg.	Clear Error
0:S.0/7	0:S.0/6	0:S.0/5	0:S.0/4	0:S.0/3	0:S.0/2	0:S.0/1	0:S.0/0
Output Enable	1st Cycle Enable	Group 5 Input	Group 4 Input	Group 3 Input	Group 2 Input	Group 1 Input	Group 0 Input

For GROUP "X" INPUT and 1ST CYCLE ENABLE see Chapter 6: Groups and Modes.

OUTPUT ENABLE

This input enables Channels that have their output anding enable bit set; those channels will be turned off when this bit is low.

CLEAR ERROR

Toggle this bit ON to clear the "Any Error" bit in the Programming Error Register (I:S.7).

Remote I/O

The Remote I/O feature permits the PL-1746 module to be used in a remote I/O rack with a 1747-ASB RIO adapter module. The RIO adapter permits the SLC processor to access only the Input and Output files of modules installed in the remote rack. To access the PL-1746's M0 file data while in the remote rack:

1. Prior to installing the PL-1746 in the remote rack, and with power off, set DIP switch 1 to OFF.
2. Using Rockwell programming software, set the PL-1746's card type is set to OTHER, with ID# 3535, M0 file length 16320, and M1 file length 16380.
3. Set up the desired input and output file register mappings as described in the Register Mapping section.

M1 File data is not accessible while the PL-1746 is operating in Remote I/O mode.

Register Mapping

Register Mapping provides an automatic way to reflect M0 File or M1 File data into any of the first eight Input File words (I:S.0 - I:S.7) and to reflect data from any of the first eight Output File words (O:S.0 - O:S.7) into the M0 File or M1 File. Register Mapping may be used with the PL-1746 operating in either Local I/O mode or Remote I/O mode; however, M1 Files may not be accessed when the PL-1746 is operating in Remote I/O mode.

To set up a mapping, enter a Mapping Index Number into the Mapping Source register for the desired Input File word or Output File word. This can be accomplished by using a PS-6400 Keypad as described in the Input Maps and Output Maps sections in chapter 4. It can also be done over the backplane, if the PL-1746 is operating in Local I/O mode. It cannot be done over the backplane if the PL-1746 is operating in Remote I/O mode, since, in that case, the RIO adapter prevents access to the PL-1746's M0 File. The Mapping Index Number for each M0 File word and each M1 File word is indicated in the Quick Reference. Entering a value of 0 as a Mapping Index Number causes the Input or Output File word to revert to it's pre-assigned meaning; those meanings are indicated in the Quick Reference.

For example, suppose that, using a PL-1746 in slot 4, it is desirable to work with Analog Output 1 via mapping, rather than directly through the M0 file. Using the PS-6400 Keypad:

- 1. Enter the value 210 as the Output Map # for Reg # 2.**
This puts the Mapping Index Number for Analog Output 1 Offset into the Mapping Source Register for Output File word 2 (O:4.2).
- 2. Enter the value 212 into the Output Map # for Reg # 3.**
This puts the Mapping Index Number for Analog Output 1 High RPM into the Mapping Source Register for Output File word 3 (O:4.3).
- 3. Enter the value 214 into the Input Map # for Reg # 2**
This puts the Mapping Index Number for Analog Output 1 Value into the Mapping Source Register for Input File word 2 (I:4.2).

The same purpose could be achieved over the backplane:

1. Move the value 210 into M0:4.193.
2. Move the value 212 into M0:4.194.
3. Move the value 214 into M0:4.210.

Now new Offset and High RPM values can be written via the Output File and read the Analog Value via the Input File.

Quick Reference

PL-1746 Quick Reference (Applies to all PL-1746 models, except as noted)

Revised 6-9-00

Notes:

1.I/O Module ID Code: Local = 13235, Remote = 3535

2.M0 file size = 16320. M1 file size = 16380.

3.Mapping Index Number for M0 file: (Address * 2) + 128.

4.Registers in the M0 file are not contiguous; space has been left between register groups for future expansion. To maintain future compatibility, SLC programs should not access unlisted registers; writes to these registers result in Illegal Function Errors.

5.In the Read/Write Capability column, R/W means Read/Write, R/O means Read-Only, W/O means Write-Only, and starred items cannot be written while the resolver/encoder is in motion.

<i>PL-1746 Function Name</i>	<i>SLC 500 File Address</i>	<i>Mapping Index Number</i>	<i>Read/Write Capability</i>	<i>Valid Range for Data</i>	<i>Reference Page</i>
Analog Outputs					
Analog Quantity (Real-World Outputs)	M0:S.40	208	R/W	0-2 Model C01	4-2
Analog Output 1 Offset	M0:S.41	210	R/O	0 Models C02,C03,C04	4-1
Analog Output 1 High RPM	M0:S.42	212	R/W	0-4095	4-1
Analog Output 1 Value	M0:S.43	214	R/O	0-3000	4-1
Analog Output 2 Offset	M0:S.44	216	R/O	0-4095	4-1
Analog Output 2 High RPM	M0:S.45	218	R/W	0-3000	4-1
Analog Output 2 Value	M0:S.46	220	R/O	0-4095	4-1
Channel Copy					
Channel Copy Source Program	M0:S.800	1728	R/W*	0-47	4-2
Channel Copy Source Channel	M0:S.802	1732	R/W*	0-31	4-2
Channel Copy Destination Program	M0:S.801	1730	R/W*	0-47	4-2
Channel Copy Destination Channel	M0:S.803	1734	R/W*	0-31	4-2
Channel Copy Command/Status	M0:S.804	1736	R/W*	Bit 15 Error Bit 14 Source Pgm Error Bit 13 Dest Pgm Error Bit 12 Source Chn Error Bit 11 Dest Chn Error Bit 10 Reserved Bits Error Bit 9 Dest Chn Not Empty Erro Bit 8-1 Reserved Bit 0 Execute/Busy	4-2
Input File					
Input Word 0 PL-1746 Output Channel 0-15 Status, 1bit/channel	I:S.0	None	R/O	0=Off 1=On	4-23
Input Word 1 PL-1746 Output Channel 16-31 Status, 1bit/channel	I:S.1	None	R/O	0=Off 1=On	4-23
Input Word 2	I:S.2	None	R/O	-32768 to 32767	3-1
Input Word 3	I:S.3	None	R/O	-32768 to 32767	3-1
Input Word 4	I:S.4	None	R/O	-32768 to 32767	3-1

Quick Reference

<i>PL-1746 Function Name</i>	<i>SLC 500 File Address</i>	<i>Mapping Index Number</i>	<i>Read/Write Capability</i>	<i>Valid Range for Data</i>	<i>Reference Page</i>
<p>Input Word 5 Hardware Status/Error Register Models C02,C03 only.</p> <p>If an error occurs in this register, it must be cleared before any further data can be written to the PL-1746 registers.</p> <p>To clear this register, toggle O:S.0/8 from 0 to 1.</p>	I:S.5	None	R/O	Bit 15 Any Error Bit 14 Reserved Bit 13 System Busy Bit 12 Power Supply Failure Bit 11 Queue Overflow Bit 10 SLC Access Timer Timeout Bit 9 SLC Fatal Error Bit 8 Pipe Overflow Bit 7 Backplane Overflow Bit 6 Resolver Failure Bit 5 NMI Without Power Failure Bit 4 Interrupt from Unused Vector Bit 3-0 Reserved	3-3
<p>Input Word 6 Error Number Register</p>	I:S.6	None	R/O	Mapping Index Number associated with error	3-3
<p>Input Word 7 Programming Error Register</p> <p>If an error occurs in this register, it must be cleared before any further data can be written to the PL-1746 registers.</p> <p>To clear this register, toggle O:S.0/8 from 0 to 1.</p>	I:S.7	None	R/O	Bit 15 Any Error Bit 14 Command Bit 13 Read-Only Bit 12 Illegal Data Bit 11 Illegal Function Bit 10 RezeroMode Bit 9 Last Group Quantity Bit 8 Offset Mode Bit 7 Too Many Timers Bit 6 Too Many Speed Comps Bit 5 Not While Running Bit 4 Bad Pulse Values Bit 3 Out of Range Bit 2 Pulse Storage Full Bit 1 No Pulse Bit 0 Pulse Overlap	3-2
<p>Input Word 8 Raw Resolver Position</p>	I:S.8	None	R/O	0-4095	3-1
Input Mapping Registers					
Input Word 0 Map #	M0:S.208	544	R/W	0-32767	4-11
Input Word 1 Map #	M0:S.209	546	R/W	0-32767	4-11
Input Word 2 Map #	M0:S.210	548	R/W	0-32767	4-11
Input Word 3 Map #	M0:S.211	550	R/W	0-32767	4-11
Input Word 4 Map #	M0:S.212	552	R/W	0-32767	4-11
Input Word 5 Map #	M0:S.213	554	R/W	0-32767	4-11
Input Word 6 Map #	M0:S.214	556	R/W	0-32767	4-11
Input Word 7 Map #	M0:S.215	558	R/W	0-32767	4-11
Interrupts					
Interrupt Enables Channels 0-31, 1bit/channel	M0:S.132- M0:S.133	392- 394	R/W	0=Disabled 1=Enabled	4-12
Interrupt Levels Channels 0-31, 1bit/channel	M0:S.128- M0:S.129	384- 386	R/W	0= Rising Edge 1= Falling Edge	4-12

Quick Reference

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Groups					
Group Quantity	M0:S.64	256	R/W*	1-6	4-20
Group Position Display	M0:S.65	258	R/W	0=EACH 1=ONE	4-10
Logic Inputs Status	M0:S.25	178	R/O	0-255	4-11
Group 0 Channel Count	M0:S.66	260	R/W*	0-32	4-20
Group 0 Mode	M0:S.82	292	R/W*	0-5	4-20
Group 0 Offset	M0:S.74	276	R/W	0 to (Scale Factor-1)	4-8, 4-20
Group 0 Position	M0:S.16	160	R/W*	0 to (Scale Factor-1)	4-8
Group 1 Channel Count	M0:S.67	262	R/W*	0-32	4-20
Group 1 Mode	M0:S.83	294	R/W*	0-5	4-20
Group 1 Offset	M0:S.75	278	R/W	0 to (Scale Factor-1)	4-8, 4-20
Group 1 Position	M0:S.17	162	R/W*	0 to (Scale Factor-1)	4-8
Group 2 Channel Count	M0:S.68	264	R/W*	0-32	4-20
Group 2 Mode	M0:S.84	296	R/W*	0-5	4-20
Group 2 Offset	M0:S.76	280	R/W	0 to (Scale Factor-1)	4-8, 4-20
Group 2 Position	M0:S.18	164	R/W*	0 to (Scale Factor-1)	4-8
Group 3 Channel Count	M0:S.69	266	R/W*	0-32	4-20
Group 3 Mode	M0:S.85	298	R/W*	0-5	4-20
Group 3 Offset	M0:S.77	282	R/W	0 to (Scale Factor-1)	4-8, 4-20
Group 3 Position	M0:S.19	166	R/W*	0 to (Scale Factor-1)	4-8
Group 4 Channel Count	M0:S.70	268	R/W*	0-32	4-20
Group 4 Mode	M0:S.86	300	R/W*	0-5	4-20
Group 4 Offset	M0:S.78	284	R/W	0 to (Scale Factor-1)	4-8, 4-20
Group 4 Position	M0:S.20	168	R/W*	0 to (Scale Factor-1)	4-8
Group 5 Channel Count	M0:S.71	270	R/O	0-32	4-20
Group 5 Mode	M0:S.87	302	R/W*	0-5	4-20
Group 5 Offset	M0:S.79	286	R/W	0 to (Scale Factor-1)	4-8, 4-20
Group 5 Position	M0:S.21	170	R/W*	0 to (Scale Factor-1)	4-8
Output Assignments					
C02,C03 only					
Output Assignments	M0:S.600-	1328-	R/W*	0-31	4-19
Outputs 0-5, 1word/output	M0:S.605	1338			
Output Enable ANDing					
Output Enable ANDing	M0:S.272-	672-	R/W	0=On	4-19
Channels 0-31, 1bit/channel	M0:S.273	674		1=Off	
Output File					
Output Word 0	O:S.0	None	W/O	Bit 16-10 Reserved	3-3, 4-11
Logic Inputs				Bit 9 Clear Shift Register (Models C02,C03 only)	
				Bit 8 Clear Error	
				Bit 7 Output Enable	
				Bit 6 First Cycle Enable	
				Bit 5 Group 5 Input	
				Bit 4 Group 4 Input	
				Bit 3 Group 3 Input	
				Bit 2 Group 2 Input	
				Bit 1 Group 1 Input	
				Bit 0 Group 0 Input	

Quick Reference

<i>PL-1746 Function Name</i>	<i>SLC 500 File Address</i>	<i>Mapping Index Number</i>	<i>Read/Write Capability</i>	<i>Valid Range for Data</i>	<i>Reference Page</i>
Output Word 1 Active Program	O:S.1	None	W/O	0-47	4-15
Output Word 2	O:S.2	None	W/O	-32768 to 32767	3-1
Output Word 3	O:S.3	None	W/O	-32768 to 32767	3-1
Output Word 4	O:S.4	None	W/O	-32768 to 32767	3-1
Output Word 5	O:S.5	None	W/O	-32768 to 32767	3-1
Output Word 6	O:S.6	None	W/O	-32768 to 32767	3-1
Output Word 7	O:S.7	None	W/O	-32768 to 32767	3-1
Output Mapping Registers					
Output Word 0 Map #	M0:S.192	512	R/W	0-32767	3-4, 4-22
Output Word 1 Map #	M0:S.193	514	R/W	0-32767	3-4, 4-22
Output Word 2 Map #	M0:S.194	516	R/W	0-32767	3-4, 4-22
Output Word 3 Map #	M0:S.195	518	R/W	0-32767	3-4, 4-22
Output Word 4 Map #	M0:S.196	520	R/W	0-32767	3-4, 4-22
Output Word 5 Map #	M0:S.197	522	R/W	0-32767	3-4, 4-22
Output Word 6 Map #	M0:S.198	524	R/W	0-32767	3-4, 4-22
Output Word 7 Map #	M0:S.199	526	R/W	0-32767	3-4, 4-22
Output Status					
Force Outputs On Channels 0-31, 1bit/channel	M0:S.256- M0:S.257	640- 642	R/W	1=Force Active 0=Force Inactive	4-23
Force Outputs Off Channels 0-31, 1bit/channel	M0:S.264- M0:S.265	656- 658	R/W	1=Force Active 0=Force Inactive	4-23
Motion ANDing/Detection					
Motion Level 1 Low Limit (ML1L)	M0:S.96	320	R/W	0 to (ML1H-1)	4-18
Motion Level 1 High Limit (ML1H)	M0:S.97	322	R/W	(ML1L+1) to 3000	4-18
Motion Level 2 Low Limit (ML2L)	M0:S.98	324	R/W	0 to (ML2H-1)	4-18
Motion Level 2 High Limit (ML2H)	M0:S.99	326	R/W	(ML2L+1) to 3000	4-18
Motion ANDing Channels 0-31, 1word/channel	M0:S.512- M0:S.543	1152- 1214	R/W*	0=OFF 1=ML1 2=ML2	4-17
Program Copy					
Program Copy Destination Program	M0:S.769	1666	R/W*	0-47	4-25
Program Copy Source Program	M0:S.768	1664	R/W*	0-47	4-25
Program Copy Command/Status	M0:S.770	1668	R/W*	Bit 15 Error Bit 14 Source Pgm Error Bit 13 Dest Pgm Error Bit 12 Reserved Bits Error Bit 11 Dest Pgm Not Empty Error Bit 10-1 Reserved Bit 0 Execute/Busy	4-25

Quick Reference

<i>PL-1746 Function Name</i>	<i>SLC 500 File Address</i>	<i>Mapping Index Number</i>	<i>Read/Write Capability</i>	<i>Valid Range for Data</i>	<i>Reference Page</i>
Program Enable					
Master Password	M0:S.106	340	R/W	0-9999	4-5
Setup Password	M0:S.105	338	R/W	0-9999	4-5
Operator Password	M0:S.104	336	R/W	0-9999	4-5
Per-Channel Operator Access Channels 0-31, 1 bit/channel	M0:S.280-	688-	R/W	0=Operator Accessible 1=Operator Inaccessible	4-5
Operator Enable Options	M0:S.107	342	R/W	Bit 15-8 Reserved Bit 7 Machine Offset Bit 6 Group Offset Bit 5 Default Program Bit 4 Motion Detect/ANDing Bit 3 Analog Outputs Bit 2 Timed Outputs Bit 1 Speed Comp Bit 0 Pulses	4-7
Pulse Copy (Creates Pulse Train)					
Pulse Copy Program	M0:S.704	1536	R/W	0-47	4-27
Pulse Copy Channel	M0:S.705	1538	R/W	0-31	4-27
Pulse Copy On (Train Start)	M0:S.706	1540	R/W	0 to (Scale Factor-1)	4-27
Pulse Copy Off (Train End)	M0:S.707	1542	R/W	0 to (Scale Factor-1)	4-27
Pulse Copy Count (Number of Pulses)	M0:S.708	1544	R/W	1 to ((Off-On)/2)	4-27
Pulse Copy Duration (of each pulse)	M0:S.709	1546	R/W	1 to ((Off-On)/2*Count)	4-27
Pulse Copy Command/Status	M0:S.710	1548	R/W*	Bit 15 Error Bit 14 Program Error Bit 13 Channel Error Bit 12 On > Scale Factor Error Bit 11 Off > Scale Factor Error Bit 10 Overlap Error Bit 9 Duration Error Bit 8 Reserved Bits Error Bit 7-1 Reserved Bit 0 Execute/Busy	4-27
Pulse Edit					
Pulse Edit Program	M0:S.896	1920	R/W	0-47	4-30
Pulse Edit Channel	M0:S.897	1922	R/W	0-31	4-30
Pulse Edit On (Leading Edge)	M0:S.898	1924	R/W	0 to Scale Factor	4-30
Pulse Edit Off (Trailing Edge)	M0:S.899	1926	R/W	0 to Scale Factor	4-30
Pulse Edit Pulse Index (within channel)	M0:S.900	1928	R/W	0 to (Pulse Quantity-1)	4-30
Pulse Edit Pulse Quantity (within channel)	M0:S.901	1930	R/O	0 to (Scale Factor/2)	4-30
Pulse Edit Command/Status	M0:S.902	1932	R/W	Bit 15 Error Bit 14 Program Error Bit 13 Channel Error Bit 12 On > Scale Factor Error Bit 11 Off > Scale Factor Error Bit 10 Pulse Index Error Bit 9 Reserved Bits Error Bit 8-5 Reserved Bit 4-1 Command (see below) Bit 0 Execute/Busy	4-30

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<i>PL-1746 Function Name</i>	<i>SLC 500 File Address</i>	<i>Mapping Index Number</i>	<i>Read/Write Capability</i>	<i>Valid Range for Data</i>	<i>Reference Page</i>
				Commands (bits 4-1): 0000 Read 0001 Write 0010 Increment On 0011 Decrement On 0100 Increment Off 0101 Decrement Off 0110 Increment Both 0111 Decrement Both 1000 Increment All 1001 Decrement All 1010 Change On 1011 Change Off 1100 Reserved 1101 Reserved 1110 Reserved 1111 Reserved	
Pulses (Bulk Pulse Storage in M1 File) Pulse Number (P is the Pulse Number.) Pulse Program/Channel Program in high byte Channel in low byte Pulse On Pulse Off	M1:S.A where A = 4 ×(P-1) M1:S.B where B = 4 ×(P-1)+1 M1:S.C where C = 4 ×(P-1)+2 M1:S.D where D = 4 ×(P-1)+3	32768+8 ×(P-1) 32768+8 ×(P-1)+2 32768+8 ×(P-1)+4 32768+8 ×(P-1)+6	R/O R/O R/O R/O	1-1252Models C01,C04 1-787Models C02,C03 Note: A pulse number 0 indicates an invalid pulse. Program: 0-47 Channel: 0-31 0 to (Scale Factor-1) 0 to (Scale Factor-1)	
Rate Display RPM Update Rate Toggle RPM Displayed Units Decimal Point Location Rate Multiplier Rate Divisor	M0:S.49 M0:S.50 M0:S.51 M0:S.52 M0:S.53 M0:S.54	226 228 230 232 234 236	R/W R/W R/W R/W R/W R/W	0=1/s 1=2/s 2=10/s 0-9999 0=RPM 1=BPM 2=CPM 3=IPM 0-3 1-1091 1-63	4-36 4-46 4-35 4-35 4-35 4-35
Resolver Direction of Rotation Machine Offset Machine Position Resolver Mode Resolver Position Resolver Speed Scale Factor	M0:S.34 M0:S.33 M0:S.24 M0:S.60 M0:S.23 M0:S.22 M0:S.32	196 194 176 248 174 172 192	R/W* R/W* R/W* R/W* (-C01) R/O R/O R/W*	0=CCW 1=CW 0 to (Scale Factor-1) 0 to (Scale Factor-1) 0=Master 1=Slave R/O models C02,C03, C04 (set via DIP Switch) 0 to (Scale Factor-1) 0-3000 2-4096 Resolver-Based Units (-R in model #) 2-4000 Encoder-Based Units (-E in model #)	4-4 4-14 4-14 4-36 4-14 4-15 4-37

Quick Reference

<i>PL-1746 Function Name</i>	<i>SLC 500 File Address</i>	<i>Mapping Index Number</i>	<i>Read/Write Capability</i>	<i>Valid Range for Data</i>	<i>Reference Page</i>
Shift Register Models C02,C03 only					
Shift Position	M0:S.917	1962	R/W	0 to (Scale Factor-1)	4-39
Window On	M0:S.918	1964	R/W	0 to (Scale Factor-1)	4-39
Window Width	M0:S.919	1966	R/W	0 to (Scale Factor-1)	4-39
Program 0 Shift Counts (Channels 0-31)	M0:S.920- M0:S.951	1968- 2030	R/W	0-255	4-39
Program 1 Shift Counts (Channels 0-31)	M0:S.952- M0:S.983	2032- 2094	R/W	0-255	4-39
Program 2 Shift Counts (Channels 0-31)	M0:S.984- M0:S.1015	2096- 2158	R/W	0-255	4-39
Program 3 Shift Counts (Channels 0-31)	M0:S.1016- M0:S.1047	2160- 2222	R/W	0-255	4-39
Program 4 Shift Counts (Channels 0-31)	M0:S.1048- M0:S.1079	2224- 2286	R/W	0-255	4-39
Program 5 Shift Counts (Channels 0-31)	M0:S.1080- M0:S.1111	2288- 2350	R/W	0-255	4-39
Program 6 Shift Counts (Channels 0-31)	M0:S.1112- M0:S.1143	2352- 2414	R/W	0-255	4-39
Program 7 Shift Counts (Channels 0-31)	M0:S.1144- M0:S.1175	2416- 2478	R/W	0-255	4-39
Program 8 Shift Counts (Channels 0-31)	M0:S.1176- M0:S.1207	2480- 2542	R/W	0-255	4-39
Program 9 Shift Counts (Channels 0-31)	M0:S.1208- M0:S.1239	2544- 2606	R/W	0-255	4-39
Program 10 Shift Counts (Channels 0-31)	M0:S.1240- M0:S.1271	2608- 2670	R/W	0-255	4-39
Program 11 Shift Counts (Channels 0-31)	M0:S.1272- M0:S.1303	2672- 2734	R/W	0-255	4-39
Program 12 Shift Counts (Channels 0-31)	M0:S.1304- M0:S.1335	2736- 2798	R/W	0-255	4-39
Program 13 Shift Counts (Channels 0-31)	M0:S.1336- M0:S.1367	2800- 2862	R/W	0-255	4-39
Program 14 Shift Counts (Channels 0-31)	M0:S.1368- M0:S.1399	2864- 2926	R/W	0-255	4-39
Program 15 Shift Counts (Channels 0-31)	M0:S.1400- M0:S.1431	2928- 2990	R/W	0-255	4-39
Program 16 Shift Counts (Channels 0-31)	M0:S.1432- M0:S.1463	2992- 3054	R/W	0-255	4-39
Program 17 Shift Counts (Channels 0-31)	M0:S.1464- M0:S.1495	3056- 3118	R/W	0-255	4-39
Program 18 Shift Counts (Channels 0-31)	M0:S.1496- M0:S.1527	3120- 3182	R/W	0-255	4-39
Program 19 Shift Counts (Channels 0-31)	M0:S.1528- M0:S.1559	3184- 3246	R/W	0-255	4-39
Program 20 Shift Counts (Channels 0-31)	M0:S.1560- M0:S.1591	3248- 3310	R/W	0-255	4-39
Program 21 Shift Counts (Channels 0-31)	M0:S.1592- M0:S.1623	3312- 3374	R/W	0-255	4-39
Program 22 Shift Counts (Channels 0-31)	M0:S.1624- M0:S.1655	3376- 3438	R/W	0-255	4-39
Program 23 Shift Counts (Channels 0-31)	M0:S.1656- M0:S.1687	3440- 3502	R/W	0-255	4-39
Program 24 Shift Counts (Channels 0-31)	M0:S.1688- M0:S.1719	3504- 3566	R/W	0-255	4-39

Quick Reference

<i>PL-1746 Function Name</i>	<i>SLC 500 File Address</i>	<i>Mapping Index Number</i>	<i>Read/Write Capability</i>	<i>Valid Range for Data</i>	<i>Reference Page</i>
Program 25 Shift Counts (Channels 0-31)	M0:S.1720- M0:S.1751	3568- 3630	R/W	0-255	4-39
Program 26 Shift Counts (Channels 0-31)	M0:S.1752- M0:S.1783	3632- 3694	R/W	0-255	4-39
Program 27 Shift Counts (Channels 0-31)	M0:S.1784- M0:S.1815	3696- 3758	R/W	0-255	4-39
Program 28 Shift Counts (Channels 0-31)	M0:S.1816- M0:S.1847	3760- 3822	R/W	0-255	4-39
Program 29 Shift Counts (Channels 0-31)	M0:S.1848- M0:S.1879	3824- 3886	R/W	0-255	4-39
Program 30 Shift Counts (Channels 0-31)	M0:S.1880- M0:S.1911	3888- 3950	R/W	0-255	4-39
Program 31 Shift Counts (Channels 0-31)	M0:S.1912- M0:S.1943	3952- 4014	R/W	0-255	4-39
Program 32 Shift Counts (Channels 0-31)	M0:S.1944- M0:S.1975	4016- 4078	R/W	0-255	4-39
Program 33 Shift Counts (Channels 0-31)	M0:S.1976- M0:S.2007	4080- 4142	R/W	0-255	4-39
Program 34 Shift Counts (Channels 0-31)	M0:S.2008- M0:S.2039	4144- 4206	R/W	0-255	4-39
Program 35 Shift Counts (Channels 0-31)	M0:S.2040- M0:S.2071	4208- 4270	R/W	0-255	4-39
Program 36 Shift Counts (Channels 0-31)	M0:S.2072- M0:S.2103	4272- 4334	R/W	0-255	4-39
Program 37 Shift Counts (Channels 0-31)	M0:S.2104- M0:S.2135	4336- 4398	R/W	0-255	4-39
Program 38 Shift Counts (Channels 0-31)	M0:S.2136- M0:S.2167	4400- 4462	R/W	0-255	4-39
Program 39 Shift Counts (Channels 0-31)	M0:S.2168- M0:S.2199	4464- 4526	R/W	0-255	4-39
Program 40 Shift Counts (Channels 0-31)	M0:S.2200- M0:S.2231	4528- 4590	R/W	0-255	4-39
Program 41 Shift Counts (Channels 0-31)	M0:S.2232- M0:S.2263	4592- 4654	R/W	0-255	4-39
Program 42 Shift Counts (Channels 0-31)	M0:S.2264- M0:S.2295	4656- 4718	R/W	0-255	4-39
Program 43 Shift Counts (Channels 0-31)	M0:S.2296- M0:S.2327	4720- 4782	R/W	0-255	4-39
Program 44 Shift Counts (Channels 0-31)	M0:S.2328- M0:S.2359	4784- 4846	R/W	0-255	4-39
Program 45 Shift Counts (Channels 0-31)	M0:S.2360- M0:S.2391	4848- 4910	R/W	0-255	4-39
Program 46 Shift Counts (Channels 0-31)	M0:S.2392- M0:S.2423	4912- 4974	R/W	0-255	4-39
Program 47 Shift Counts (Channels 0-31)	M0:S.2424- M0:S.2455	4976- 5038	R/W	0-255	4-39
Speed Compensation					
Speed Comp Mode	M0:S.35	198	R/W	0=ONE 1=L/T	4-45
Leading Edge Channels 0-31, 1word/channel	M0:S.384- M0:S.415	896- 958	R/W	-999.9 to 999.9	4-44
Trailing Edge Channels 0-31, 1word/channel	M0:S.448- M0:S.479	1024- 1086	R/W	-999.9 to 999.9	4-44

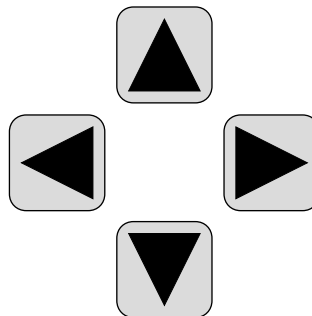
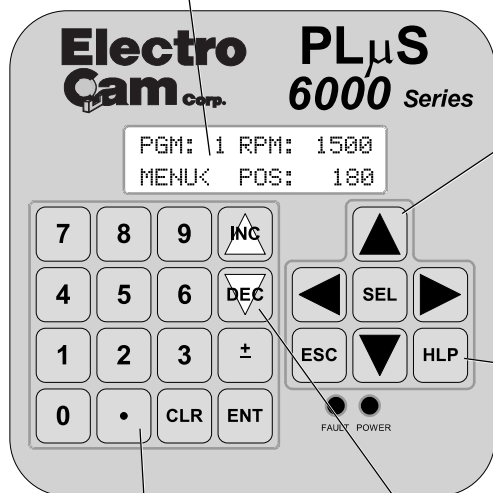
Quick Reference

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System					
Model	M0:S.0	128	R/O	1746	4-17
Options	M0:S.2	132	R/O	0 = Standard, 1 = Shift Register	4-17
Base Revision	M0:S.4	136	R/O	0-32767	4-43
Major Revision	M0:S.3	134	R/O	0-32767	4-43
Keyboard Quantity	M0:S.48	224	R/W	0-2	4-13
Rack Quantity	M0:S.56	240	R/W	0-2 Model C01 0 Models C02,C03,C04	4-34
Default Program	M0:S.120	368	R/W	0-47	4-4
EEPROM Checksum Models C02,C03 only	M0:S.5	138	R/O	-32768 to 32767	4-5
EEPROM Checksum Command/Status Models C02,C03 only	M0:S.6	140	R/W	0=Done 1=Execute/Busy	4-5
Output Quantity	M0:S.1	130	R/O	32	
Pulses Total	M0:S.26	180	R/O	1252 Units without Shift Register (no -S in model #) 787 Units with Shift Register (-S in model #)	4-29
Pulses Used	M0:S.27	182	R/O	0 to Pulses Total	4-29
Backplane Interlock	M0:S.866	1860	R/W	0=Done 1=Execute/Busy	3-1
Timed Outputs					
Time (ms) Channels 0-31, 1 word/channel	M0:S.320- M0:S.351	768- 830	R/W	0-9999	4-45

PS-6400 Keypad Overview

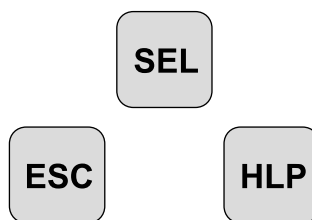
Main Screen

- Shows Active Program, RPM, Position, and Group # (if applicable).
- See **MAIN SCREEN** Section for details.
- Press **SEL** key when cursor is on “MENU” to enter Menu Tree and initiate programming.



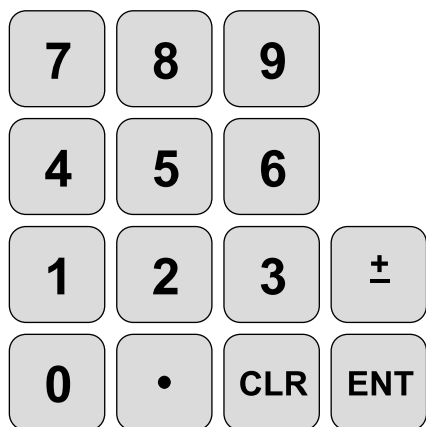
Cursor Keys

- Scroll through Menu Tree.
- Move around **within a screen**.
- Scroll through pulses.



ESC, SEL, HLP Keys

- **ESC** exits from current menu level to previous menu, or aborts numeric entry.
- **SEL** enters a new menu level; toggles a value; and selects an output group if multiple groups are used.
- **HLP** shows help regarding menu selection and what keys to press. **Use this key if unsure what to do.**



INC, DEC Keys

- Increment or decrement a value **within a field**.
- Hold for rapid scrolling of value.

Numeric Keys

- Input numeric values within a field.
- **ENT must be pressed to enter the value**; entry will flash until ENT is pressed.
- **CLR** will backspace within an entry.
- ± will convert a positive number to a negative number, or vice versa.

Menu Tree

Functions are listed alphabetically in Chapter 4.

